WHAT IS CLAIMED IS:

1. An input buffer circuit to/from which first and second input signals are inputted and first and second output signals are outputted, wherein

said input buffer circuit comprises:

a first differential amplifier circuit;

a first integration circuit to which said first output signal is inputted;

a second integration circuit to which said second output signal is inputted; and

a first voltage converting circuit converting a voltage value outputted from said first and second integration circuits, respectively, and

said first differential amplifier circuit includes:

a first transistor including a gate to which said first input signal is inputted; and

a second transistor including a gate to which said second input signal is inputted, and

an output of said first voltage converting circuit is connected with respective back gates of said first and second transistors.

2. The input buffer circuit according to claim 1, wherein

said input buffer circuit further comprises a second differential amplifier circuit which is in a cascade connection with said first differential amplifier circuit, and

said second differential amplifier circuit includes:

a third transistor including a gate to which a third output signal outputted from said first differential amplifier circuit is inputted; and

a fourth transistor including a gate to which a fourth output signal outputted from said first differential amplifier circuit is inputted, and

said output of said first voltage converting circuit is further connected with respective back gates of said third and fourth transistors.

3. The input buffer circuit according to claim 1, wherein

said input buffer circuit further comprises:

a second differential amplifier circuit which is in a cascade connection with said first differential amplifier circuit; and

a second voltage converting circuit converting said voltage value outputted from said first and second integration circuits, respectively, and

said second differential amplifier circuit includes:

a third transistor including a gate to which a third output signal outputted from said first differential amplifier circuit is inputted; and

a fourth transistor including a gate to which a fourth output signal outputted from said first differential amplifier circuit is inputted, and

an output of said second voltage converting circuit is connected with respective back gates of said third and fourth transistors.

4. The input buffer circuit according to claim 1, wherein

said first differential amplifier circuit further comprises a constant current source including a fifth transistor connected with said first transistor and a sixth transistor connected with said second transistor, and

said output of said first voltage converting circuit is further connected with respective back gates of said fifth and sixth transistors.